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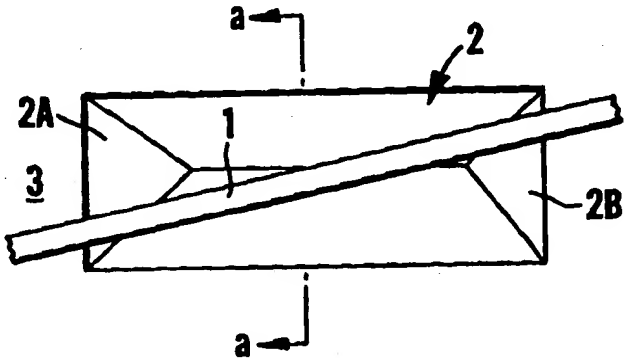
(54) Title: THERMALLY ISOLATED SILICON LAYER

(57) Abstract

An integrated optical circuit is formed in a silicon layer and supported on a substrate (5), a portion (1) of the silicon layer is substantially thermally isolated from the substrate (5) by extending over a recess (2) in the substrate (5), e.g. in the form of a bridge. Temperature control means (9) are provided to control the temperature of the said portion (1) of the silicon layer or of a device provided thereon. A thermal expansion gap (1A) may be provided in the said portion (1) to accommodate thermal expansion of the said portion (1) relative to the substrate (5).



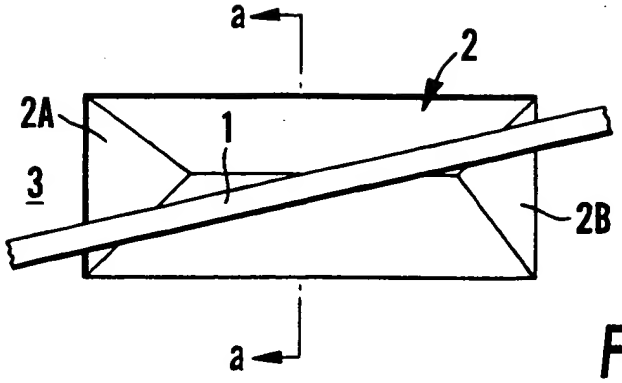


Fig.1

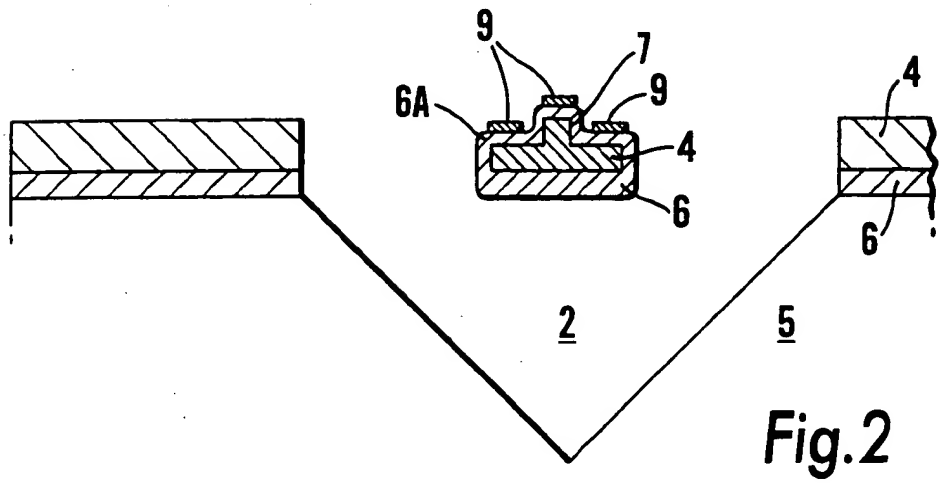


Fig.2

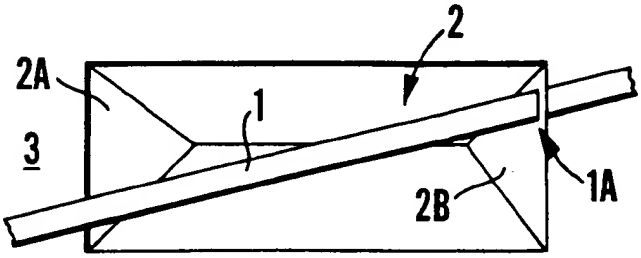


Fig.3

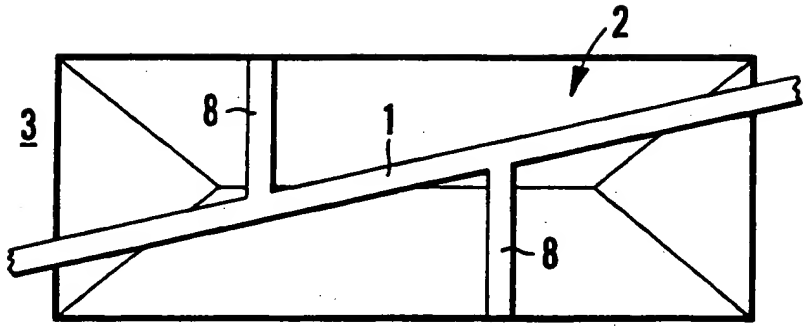


Fig.4

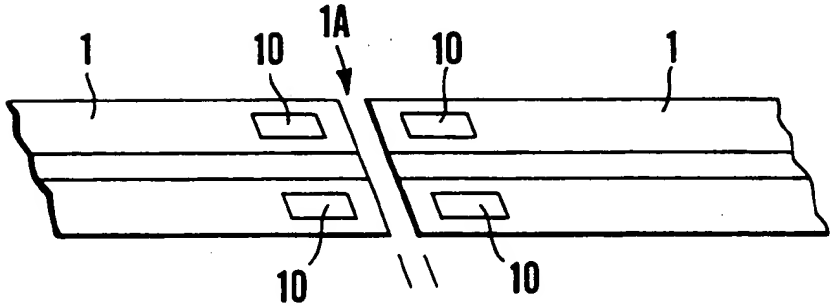


Fig.5

THERMALLY ISOLATED SILICON LAYER

TECHNICAL FIELD

This invention relates to an integrated optical circuit formed in a silicon layer and supported on a substrate with at least a portion of the silicon layer being substantially thermally isolated from the substrate.

BACKGROUND ART

Temperature control of integrated optical devices, particularly silicon-on-insulator (SOI) waveguides, is desirable in order to adjust the refractive index of the device (the refractive index of silicon increases by a factor of 2×10^{-4} per degree C. which is a relatively large change compared to other optical materials).

Prior art such as EP-A-0255270 proposes the use of a recess in a silicon substrate in order to thermally isolate a silica waveguide extending thereover to avoid thermal stresses in the waveguide due to the different thermal expansion co-efficients of silicon and silica. This prior art also discloses forming the waveguide as a cantilever structure to provide an on-off switch activated by displacement of the cantilevered waveguide.

The present invention is concerned with integrated optical circuits formed in a silicon layer.

DISCLOSURE OF INVENTION

According to a first aspect of the invention, there is provided an integrated optical circuit formed in a silicon layer and supported on a substrate, a portion of the silicon layer being substantially thermally isolated from the substrate by extending over a recess in the substrate and temperature control means being provided to control the temperature of the said portion of the silicon layer or of a device provided thereon.

Preferred and optional features of the invention will be apparent from the subsidiary claims of the specification.

BRIEF DESCRIPTION OF DRAWINGS

The invention will now be further described, merely by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a plan view of a silicon-on-insulator waveguide extending across a recess in a substrate according to a first embodiment of the invention;

Figure 2 shows a cross-sectional view taken on line a-a of Figure 1;

Figure 3 is a similar view to Figure 1 and shows a second embodiment of the device;

Figure 4 is a similar view to Figure 1 and shows a third embodiment of the device; and

Figure 5 shows an enlarged view of part of the device of Figure 3.

BEST MODE FOR CARRYING OUT THE INVENTION

The integrated optical circuit described herein is based on a silicon-on-insulator (SOI) chip. A process for forming this type of chip is described in a paper entitled "Reduced defect density in silicon-on-insulator structures formed by oxygen implantation in two steps" by J. Morgail et al. Appl. Phys. Lett., 54, p526, 1989. This describes a process for forming a Very Large Scale Integrated (VLSI) silicon-on-insulator wafer. The silicon layer of such a wafer is then increased, e.g. by epitaxial growth, to make it suitable for forming the basis of the integrated interferometer described herein. SOI chips can also be formed in other ways.

Figure 1 shows a silicon-on-insulator waveguide 1 extending across a recess 2 in a silicon substrate 3 in the form of a bridge. The recess is in the form of a V-groove etched in the substrate, the ends of the V-groove comprising sloping faces 2A, 2B due to the manner in which the V-groove is etched. The waveguide 1 extends obliquely across the V-groove 2 and forms part of an integrated optical circuit (not shown) such as a Mach-Zehnder type optical switch.

As shown in Figure 2, the device is formed on an SOI chip which comprises an upper layer of silicon 4 separated from a silicon substrate 5 by an insulator layer 6, typically formed of silicon dioxide. Further details of this form of waveguide are given in a paper entitled "Low Loss Single Mode Optical Waveguides with Large Cross-Section in Silicon-on-Insulator" by J. Schmidtchen et al in Electronic Letters. 27, p1486. 1991 and in PCT patent specification no. WO95/08787.

The SOI waveguide 1 extending across the V-groove comprises a rib waveguide 7 formed in the silicon layer 4 supported by the silicon dioxide layer 6. Figure 2 also shows the oxide coating 6A which is formed over the rib 7 and adjacent silicon slabs 4. A portion of the SOI waveguide 1 is substantially thermally isolated from the substrate 5 as it extends across a region from which areas of the substrate adjacent and beneath the waveguide have been removed during the formation of the V-groove 2. The length of the recess 9 depends on the application. Typically, the recess 9 may be between 50 and 1000 microns in length.

The formation of an SOI waveguide extending over a V-groove is also described in the applicants' co-pending application no. PCT/GB96/01608 (publication no. WO97/42534) which describes a waveguide overhanging the end of a V-groove to facilitate butt coupling with an optical fibre positioned in th V-groove.

The rib waveguide is typically 4 - 13 microns wide and 4 - 13 microns deep (measured from the oxide layer 6) and the oxide layer 6 typically has a thickness of around 0.4 microns so the overall thickness of the suspended waveguide is around 5 - 14 microns. Although the width of the rib waveguide is typically 4 - 13 microns, the slab waveguide (comprised of the silicon layer 4) on either side thereof as well as the underlying oxide layer 6 preferably have a greater width, e.g. of 20 - 40 microns, to increase the strength of the suspended waveguide.

The device shown in Figures 1 and 2 is also provided with temperature control means, e.g. in the form of a metal coating or coatings 9, typically of aluminium, applied over the waveguide 1 or a portion of the waveguide 1. As shown in Figure 2, the coating 9 may be deposited as one or more conductive strips on the slab on either side of the rib waveguide 7 and/or on the rib 7. The conductive strips can be heated by passing a current therethrough to heat the waveguide 1. Due to the thermal isolation of the waveguide 1, very little power is required to heat the waveguide 1, e.g. a few micro Watts, and its temperature can be increased very quickly, e.g. at a rate of less than a millisecond/degree C.

Other forms of temperature control means may be provided, e.g. conductive tracks formed in the slab waveguide by doping regions of the silicon layer 4.

By providing the waveguide in a substantially thermally isolated portion of the silicon layer 4, the need to heat large areas of the chip, which would consume considerably more power and be more difficult to control, is avoided.

The temperature of the waveguide 1 can be monitored by suitable temperature sensing means, e.g. one or more pn junctions formed across the waveguide 1 or other part of the thermally isolated portion of the silicon layer 4. Figure 5 shows pn junctions formed across the waveguide by means of p-doped and n-doped regions 10 formed in the silicon slab 4 on either side of the rib waveguide.

Other forms of temperature control means and temperature monitoring means may be used for heating and monitoring the temperature of the waveguide 1 or selected parts of it.

Due to the relatively high thermal expansion co-efficient of silicon (approximately $2x10^{-6}$/degree C) it may, in some circumstances, be desirable to accommodate thermal expansion of the thermally isolated portion of the silicon layer 4 extending across the recess 2 by provision of a thermal expansion gap 1A therein. Figure 3 shows an embodiment in which a gap 1A is provided in the waveguide extending across the recess 2. The gap 1A may be provided at any position along the waveguide, but for ease of fabrication it is preferably provided near or at one end of the waveguide 1 as shown in Figure 3. The gap 1A should be of sufficient size to accommodate the maximum expected thermal expansion of the waveguide but will typically need to be less than one micron wide. However, depending on the fabrication proceed used, it may in practice, be larger than required. A gap of a few microns width will have negligible effect on the transmission of light along the rib waveguide.

The ends of the waveguide 1 on each side of the gap 1A are preferably provided with an anti-reflective (AR) coating to reduce Fresnel losses to negligible levels and the facets at the ends of the waveguides on each side of the gap 1A are preferably angled relative to the perpendicular to the length of the waveguide to reduce any remaining back reflections. Figure 5A shows the angled facets provided at the ends of the waveguide 1 either side of the gap 1A.

Depending on the length of the thermally isolated portion of silicon layer 4 extending across the recess 6, and the dimensions and hence strength thereof, it may, be desirable to provide the suspended portion with localised support as it crosses the recess 2. This may comprise beams 8 formed from the silicon layer 4 together with the underlying oxide layer extending out from the sides of the V-groove to help support the suspended portion as shown in Figure 4. Other forms

of support which increase the str ngth of the thermally isolated portion of the waveguide without significantly compromising its thermal isolation may also be used.

The SOI chip described above is particularly suited to forming a suspended portion of a silicon layer as the oxide layer 6 underlying the silicon layer 4 serves to protect the silicon layer 4 from being attacked by the etchant used to form the recess 2. The use of an anisotropic etchant such as CsOH or KOH which etches silicon much faster than it etches silicon dioxide can thus be used to form the structure illustrated.

It will be appreciated that other forms of recess 2 may be used, the V-groove just being an example which is particularly easy to form. As illustrated in Figure 1, the waveguide 1 preferably extends obliquely across the V-groove 2 as if it extended parallel to the V-groove, the etching process would tend to form two parallel V-grooves either side of the waveguide rather than etching beneath the waveguide. The recess need only be of a size sufficient to provide the required thermal isolation of the waveguide 1.

The ability to thermally stabilise a waveguide and/or control its temperature and therefore properties such as its refractive index has potential use in a wide variety of applications, e.g. as a tuneable arm of an interferometer, tuneable gratings. in switches, tuneable filters etc, and particularly in applications requiring tuning over a timescale of a few milliseconds and, as mentioned above, this can be achieved using currents only in the order of milliamps.

Although the embodiment described above relates to the thermal isolation and temperature control of a waveguide extending across a recess, a similar structure may be used to thermally stabilise and/or control the temperature of other integrated optical components or devices. A device may, for instance, be supported or formed on a silicon bridge or projection analogous to that described

above, or a plurality of components or a section of an integrated circuit may likewise be provided or formed on such a structure to thermally isolate it from the surrounding structures and/or adjacent devices. In each case, the bridge or projection comprises a portion of the silicon layer 4 (together with the underlying oxide layer) which extends across or over a recess in the substrate 5. Any form of integrated optical component, device or circuit which can be formed in a silicon layer, and which can be fitted onto such a suspended portion, may likewise be formed thereon.

CLAIMS

1. An integrated optical circuit formed in a silicon layer and supported on a substrate, a portion of the silicon layer being substantially thermally isolated from the substrate by extending over a recess in the substrate and temperature control means being provided to control the temperature of the said portion of the silicon layer or of a device provided thereon.

2. An integrated optical circuit as claimed in Claim 1 in which the temperature control means comprises a metallic layer which may be heated by passing a current therethrough.

3. An integrated optical circuit as claimed in Claim 1 or 2 in which temperature sensing means are provided for monitoring the temperature of the said portion.

4. An integrated optical circuit as claimed in Claim 3 in which the temperature sensing means comprises a pn junction formed on the said portion.

5. An integrated optical waveguide as claimed in any preceding claim in which the said portion is provided with a thermal expansion gap to accommodate differential thermal expansion of the said portion relative to the substrate.

6. An integrated optical circuit as claimed in Claim 5 in which the gap is provided near or at one end of the said portion.

7. An integrated optical circuit as claimed in any preceding claim provided with one or more supports for supporting the said portion as it extends over the recess.

8. An integrated optical circuit as claimed in Claim 7 in which the support comprises a beam extending from an edge of the recess to the said portion.

9. An integrated optical circuit as claimed in any preceding claim in which an integrated waveguide, formed in the silicon layer, is provided on the said portion.

10. An integrated optical circuit as claimed in Claim 9 in which the waveguide comprises a silicon rib waveguide.

11. An integrated optical circuit as claimed in Claims 5 and 9 in which the waveguide is provided with angled facets on each side of the gap to reduce back-reflections therefrom.

12. An integrated optical circuit as claimed in Claim 5 and 9 or Claim 11 in which the ends of the waveguide on either side of the gap are provided with an anti-reflective coating.

13. An integrated optical circuit as claimed in any preceding claim in which the said portion has a length in the range 50 to 1000 microns.

14. An integrated optical circuit as claimed in any preceding claim in which the said portion has a width of up to 40 microns and a thickness of up to 14 microns.

15. An integrated optical circuit as claimed in any preceding claim in which the recess comprises a V-groove.

16. An integrated optical circuit as claimed in any preceding claim formed from a silicon-on-insulator chip.

17. An integrated optical circuit substantially as her inbefor described with reference to the accompanying drawings.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 98/01105

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G02B6/12 G02F1/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G02B G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SUGITA A ET AL: "BRIDGE-SUSPENDED SILICA-WAVEGUIDE THERMO-OPTIC PHASE SHIFTER AND ITS APPLICATION TO MACH-ZEHNDER TYPE OPTICAL SWITCH" TRANSACTIONS OF THE INSTITUTE OF ELECTRONICS, INFORMATION AND COMMUNICATION ENGINEERS OF JAPAN, vol. E73, no. 1, 1 January 1990, pages 105-108, XP000103975	1,2, 7-12,15, 16
Y	see page 106, paragraph 2.2 - paragraph 3.1; figures 3,6	5,6,13, 14

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 July 1998	29/07/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wahl, M

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 426 (P-935), 22 September 1989 -& JP 01 158413 A (NIPPON TELEGR & TELEPH CORP), 21 June 1989, see abstract	1,2,9,16
Y		5,6,13, 14
Y	WU S ET AL: "INTEGRATED OPTICAL SENSORS USING MICROMECHANICAL BRIDGES AND CANTILEVERS" INTEGRATED OPTICS AND MICROSTRUCTURES, BOSTON, SEPT. 8 - 9, 1992, no. CONF. 1, 8 September 1992, MASSOOD TABIB-AZAR;POLLA D A (EDS), pages 83-89, XP000652415 see abstract; figures 1,3 see page 83, line 25 - page 85, line 8	5,6,13, 14
Y	EP 0 255 270 A (NIPPON TELEGRAPH & TELEPHONE) 3 February 1988 cited in the application see figures 18-21; examples 17-20	5,6
Y	PATENT ABSTRACTS OF JAPAN vol. 012, no. 072 (E-588), 5 March 1988 -& JP 62 213288 A (OKI ELECTRIC IND CO LTD), 19 September 1987, see abstract	5,6

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 98/01105

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